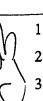


What is claimed is:

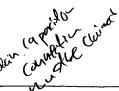
- 1 1. A noise reduction device comprising:
- a complementary metal-oxide semiconductor (CMOS) transistor operable as a
- 3 two-terminal device in a depletion mode and having a non-linear voltage variation for
- 4 charge being removed at a constant rate, the CMOS transistor is formed in an n-type
- substrate having an n-type drain, an n-type source, an p-type polysilicon gate, and a gate
- 6 oxide layer.
- 1 2. The noise reduction device of claim 1, wherein the non-linear voltage variation is
- 2 given by:

$$v_2(t) = Vcc + \frac{aCo}{K} - \sqrt{\left(\frac{aCo}{K}\right)^2 - \frac{2It}{K}}$$

- 1 3. The noise reduction device of claim 2, wherein the gate oxide layer has a
- 2 thickness of between about twenty and forty angstroms.



- 4. A circuit comprising:
- a voltage node;
 - a ground node; and
- 4 a transistor coupled between the voltage node and the ground node, the transistor
- 5 including an p-type polysilicon gate is capable of decreasing noise signals above an
- 6 absolute value of an operating voltage value at the voltage node and increasing noise
- 7 signals below the absolute value of the operating voltage value.



5. The circuit of claim 4, wherein the operating voltage value is between about .5 volts and about 1.5 volts.



1 2 3	6.	The circuit of claim 5, further comprising: a logic cell coupled to the voltage node and located in close proximity to the tor.
1	7.	A circuit comprising:

2 an energy source;

a processor having a plurality of notices coupled to the energy source and forming

a power supply grid having a number of resonant frequencies; and

a number of transistors coupled to at least one of the plurality of nodes such that

at least one of the number of transistors is operable as a voltage variable capacitor capable

7 of reducing the amplitude of resonant frequencies.

8. The circuit of claim 7, wherein the number of transistors is greater than about ten

2 thousand.

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9. A circuit comprising:

a die having a high voltage node and a low voltage node; and

a transistor coupled between the high voltage node and the low voltage node and

operable for controlling a voltage at the low voltage node.

1 10. The circuit of claim 9, wherein the transistor has a gate, a drain, and a source, and

2 the gate is coupled to the high voltage node and the source and the drain are coupled to

3 the low voltage node.

- 1 11. A circuit comprising:
- 2 a substrate;
- a load fabricated on the substrate;
- an energy source coupled to the load, the energy source having an operating
- 5 voltage and a unidirectional noise signal; and

6		an electronic device fabricated on the substrate and coupled to the load, the	
7	electr	electronic device is capable of reducing the unidirectional noise signal more than a fixed	
8	capac	capacitor having a capacitance value equal to the capacitance value of the electronic	
9	devic	device operating at the operating voltage.	
1	12.	The circuit of claim 11, wherein the electronic device is a voltage variable	
2	capac	itor.	
1	13.	The circuit of claim 11, wherein the electronic device is a MOSFET.	
		/	
1	14.	A circuit comprising:	
2		a die;	
3		a ground node located on the die;	
4		a voltage node located on the die; and	
5		an electronic device coupled between the ground node and the voltage node and	
6	capab	le of providing an asymmetrical response to incremental voltage variations about an	
7	opera	operational node voltage at the voltage node.	
1		Meda come or	
4	15.	The circuit of claim 14, wherein incremental voltage variations of one polarity	
2	are da	amped and incremental voltage variations of the opposite polarity are amplified.	
1	16.	The circuit of claim 14, wherein the bias node voltage is about 1.3 volts.	
'	10.	- Chence of column 1., wherein the <u>orange</u> note of change is a column to the change is a column to column to the change is a column to column to the change is a column to the change is a column to th	
1	17.	An integrated circuit comprising:	
2	11.	a die;	
3		a processor having a plurality of cells formed on the die; and	
9		- kind and and a kind - Kill and a state of the state of	

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capable of damping positive voltage variations at the cell and amplifying negative voltage

a number of electronic devices coupled to at least one of the plurality of cells and

- 1 18. The integrated circuit of claim 17, wherein the plurality of cells are fabricated using a complementary metal-oxide semiconductor manufacturing process.
- 1 19. A method comprising:
- receiving an energy signal having a noise component at a cell formed on a die;
- 3 and
- filtering the energy signal to form a filtered energy signal by decoupling the cell
- 5 with a voltage variable capacitor.
- 1 20. The method of claim 19, wherein receiving an energy signal having a noise
- 2 component at a cell comprises:
- 3 receiving a power supply signal at the cell.
- 1 21. The method of claim 19, wherein filtering the energy signal to form a filtered
- 2 energy signal by decoupling the cell with a voltage variable capacitor comprises:
- 3 filtering the energy signal with at least one-hundred CMOS transistors operating
- 4 in the depletion-accumulation region.
- 1 22. The method of claim 19, further comprising:
- 2 configuring at least one of the number of electronic devices to have a drain, a
- 3 source, and a bulk connection coupled to a high voltage level and a gate coupled to a low
- 4 voltage level.
- 1 23. A method comprising:
- 2 adding a number of electronic devices having a voltage variable capacitance to an
- 3 electronic grid to suppress resonant frequencies in the electronic grid.
- 1 24. The method of claim 23, wherein adding a number of electronic devices
- 2 comprises:
- 3 selecting an active electronic device; and

- coupling the active electronic device between a high voltage level and a low voltage level at a logic cell.
- 1 25. The method of claim 23, further comprising:
- 2 locating at least one of the number of electronic devices between a logic cell and a
- 3 decoupling capacitor.
- 1 26. A method comprising:
- 2 transforming a resonant frequency on a power supply grid network resonant at the
- 3 resonant frequency to a higher frequency.
- 1 27. The method of claim 26, wherein transforming a resonant frequency on a power
- supply grid network resonant at the resonant frequency to a higher frequency comprises:
- adding a voltage variable capacitor to the power supply grid network.
- 1 28. The method of claim 27, further comprising:
- 2 adding a plurality of CMOS transistors configured to operate in the depletion-
- 3 accumulation region to the power supply grid network.